CLAIMS

1. A two layer LTO backside seal for a wafer having a first major side and a second major side comprising:

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent of one major side of the wafer; and

a high stress LTO layer having a first major side and second major side, the first major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

2. A wafer according to claim 1 further including a layer of polysilicon between the wafer and the low stress layer.

3. A method of forming a two layer LTO backside seal on a wafer having two major sides including the steps of:

forming a low stress LTO layer having a first major side and second major side with the first major side on one major side of the wafer, and

forming a high stress LTO layer with a first major side and second major side with one major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

4. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 3 further including the step of forming the low stress LTO layer using high frequency RF power.

5. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 4 wherein the power of the high frequency RF is between 200 and 1600 watts.

6. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 4 or claim 5 wherein power of the high frequency RF is between 300 and 1200 watts.

7. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 4 to 6 wherein the high frequency used in forming the low stress LTO layer is about 13.56MHz.

8. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 7 further including the step of forming the low stress LTO layer using low pressure.

9. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 8 wherein the pressure used to form the low stress LTO layer is between 200 and 467 Pa.

10. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 9 further including the step of forming the low stress LTO layer using high silane flow rate.

11. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 10 wherein the silane flow used to form the low stress LTO layer is between 50 and 1000 sccm.

12. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 10 or claim 11 wherein the silane flow used to form the low stress LTO layer is between 100 and 600 sccm.

13. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 12 further including the step of forming the low stress LTO layer using temperature between 250 and 600°C.

14. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 13 wherein the temperature used to form the low stress LTO layer is between 300 and 450°C.

15. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 14 further including the step of forming the low stress LTO layer in the presence of N_2 with flow rate between 800 and 7000 sccm.

16. A method of forming a two layer LTO backside seal on a wafer as claimed in claim15 wherein the N_2 flow rate used in the formation of the low stress LTO layer is between 1000 and 4000 sccm.

17. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 16 further including the step of forming the low stress LTO layer in the presence of N_2O with flow rate between 2000 and 18000 sccm.

18. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 17 wherein the N_2O flow rate used in the formation the low stress LTO layer is between 3000 and 15000 sccm.

19. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 18 further including the step of forming the high stress LTO layer using high frequency RF power at high power.

20. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 19 wherein the power of the high frequency RF is between 200 and 1600 watts.

21. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 19 or claim 20 wherein the power of the high frequency RF is between 300 and 1200 watts.

22. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 19 to 21 wherein the high frequency used in forming the high stress LTO layer is 13.56 MHz.

23. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 22 further including the step of forming the high stress LTO layer using low frequency RF at high power.

24. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 23 wherein the high stress LTO layer is formed using low frequency RF with power between 0 and 800 watts.

25. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 23 or claim 24 wherein the high stress LTO layer is formed using low frequency RF with power between 100 and 600 watts.

26. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 22 to 25 wherein the low frequency used in forming the high stress LTO layer is between 100 and 600 kHz.

27. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 26 wherein the low frequency used in forming the high stress LTO layer is 200 kHz.

28. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 27 further including the step of forming the high stress LTO layer using high pressure.

29. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 28 further including the step of forming the high stress LTO layer using higher pressure than the pressure used to form the low stress LTO layer.

30. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 28 or 29 wherein the pressure used to form the high stress LTO layer is between 200 and 467 Pa.

31. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 30 further including the step of forming the high stress LTO layer using low silane flow.

32. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 31 wherein the high stress LTO layer is formed using silane flow between 50 and 1000 sccm.

33. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 31 or claim 32 wherein the high stress LTO layer is formed using silane flow between 100 and 600 sccm.

34. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 31 to 33 wherein the high stress LTO layer is formed using silane flow with a slower flow rate than that used in the step of forming the low stress LTO layer.

35. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 34 further including the step of forming the high stress LTO layer using at least one temperature between 250 and 600°C.

36. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 35 wherein the temperature used to form the high stress LTO layer is between 300 and 450°C.

37. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 36 further including the step of forming the high stress LTO layer in the presence of N_2 with a flow rate between 800 and 7000 sccm.

38. A method of forming a two layer LTO backside seal on a wafer as claimed in 37 wherein the N_2 flow rate used in the formation of the high stress LTO layer is between 1000 and 4000 sccm.

39. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 38 further including the step of forming the high stress LTO layer in the presence of N_2O with a flow rate between 2000 and 18000 sccm.

40. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 39 wherein the N_2O flow rate used in the formation of the high stress LTO layer is between 3000 and 15000 sccm.

41. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 40 wherein the steps of forming the low stress and high stress LTO layers include the step of forming a network between the low stress and high stress layers.

42. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 41 wherein the wafer is a p-type silicon wafer.

43. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 3 to 41 wherein the wafer is an n-type silicon wafer.

44. A wafer formed using the method according to any of claims 3 to 43.

45. A pp+ silicon epitaxial wafer including:

a p+ substrate a first major side and a second major side,

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the p+ substrate, and

a high stress LTO silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.

46. An nn+ silicon epitaxial wafer including:

an n+ substrate a first major side and a second major side,

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the n+ substrate, and

a high stress LTO silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.